CLAIMS

What is claimed is:

1. A method for look-ahead load pre-fetch, comprising the steps of:

searching an instruction stream for a load memory instruction while the instruction stream is stalled waiting for completion of a previous instruction in the instruction stream;

issuing a pre-fetch operation for the load memory instruction.

2. The method of claim 1, wherein the previous instruction is a previous load memory instruction.

3. The method of claim 1, wherein the step of issuing comprises the step of issuing the pre-fetch operation if a memory address for the load memory instruction is resolved and not otherwise.

4. The method of claim 1, wherein the step of issuing the pre-fetch operation comprises the step of issuing the pre-fetch operation while the instruction stream is stalled on the previous instruction.

5. The method of claim 1, wherein the pre-fetch operation reads a set of data from a main memory and stores the data in a cache.

6. The method of claim 1, further comprising the steps of searching the instruction stream for a set of additional load memory instructions and issuing a

pre-fetch operation for each additional load memory instruction having a memory address which is resolved while the instruction stream is stalled.

7. An apparatus for look-ahead load pre-fetch, comprising:

means for searching an instruction stream for a load memory instruction while the instruction stream is stalled waiting for completion of a previous instruction in the instruction stream;

means for issuing a pre-fetch operation for the load memory instruction.

8. The apparatus of claim 7, wherein the previous instruction is a previous load memory instruction.

9. The apparatus of claim 7, wherein the means for issuing comprises means for issuing the pre-fetch operation if a memory address for the load memory instruction is resolved and not otherwise.

10. The apparatus of claim 7, wherein the means for issuing the pre-fetch operation comprises means for issuing the pre-fetch operation while the instruction stream is stalled on the previous instruction.

11. The apparatus of claim 7, wherein the pre-fetch operation reads a set of data from a main memory and stores the data in a cache.

12. The apparatus of claim 7, further comprising means for searching the instruction stream for a set of additional load memory instructions and means for

issuing a pre-fetch operation for each additional load memory instruction having a memory address which is resolved while the instruction stream is stalled.

13. A processor, comprising:

instruction pipeline for executing an instruction stream;

means for searching the instruction pipeline for a load memory instruction while the instruction pipeline is stalled;

functional unit that issues a pre-fetch operation for the load memory instruction.

14. The processor of claim 13, wherein the instruction pipeline searches the instruction pipeline during a stall on a load memory instruction in the instruction stream.

15. The processor of claim 13, wherein the functional unit issues the pre-fetch operation if a memory address for the load memory instruction is resolved and not otherwise.

16. The processor of claim 13, wherein the functional unit issues the pre-fetch operation while the instruction stream is stalled.

17. The processor of claim 13, further comprising a cache such that the pre-fetch operation reads a set of data from a main memory and stores the data in the cache.